	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	487843	bias ner40 eeprom	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:03	
2	BRS	L2	520	(bias ner40 eeprom) near25 (block near2 cell$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:04	
3	BRS	L3	3	(bias ner40 eeprom) near25 (block near2 cell$1) near30 (page near2 cell$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:04	
4	BRS	L4	2	(bias ner40 eeprom) near25 (block near2 cell$1) near30 (page near2 cell$1) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:07	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L6	2	(bias) near25 (block near2 cell$1) near30 (page near2 cell$1) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:07	
6	BRS	L5	7	(bias ner40 eeprom) near25 (block near2 cell$1) near30 (page) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:10	
7	BRS	L7	2	(bias near40 eeprom) near25 (block near2 cell$1) near30 (page) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:11	
8	BRS	L8	2	(bias) near25 (block near2 cell$1) near30 (page) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:11	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	32	(bias) near25 (block near2 cell$1) near30 (eras$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:11	
10	BRS	L10	2	(bias) near25 (block near2 cell$1) near30 (eras$3) near40 (vt or threshold)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 17:12	
11	BRS	L11	296	(block near3 cell$1) near30 (eras$3) near40 (vt or threshold)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 18:26	
12	BRS	L12	7	(block near3 cell$1) near30 (eras$3) near40 (vth or threshold) near50 (page or sector)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/22 18:27	

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	☐	☐	US 20040029335 A1	Novel set of three level concurrent word line bias conditions for a NOR type flash memory array	438/200	58	20040212
2	☐	☐	US 20040027894 A1	Novel set of three level concurrent word line bias conditions for a NOR type flash memory array	365/202	58	20040212
3	☐	☐	US 6556481 B1	3-step write operation nonvolatile semiconductor one-transistor, nor-type flash EEPROM memory cell	365/185.24	16	20030429
4	☐	☐	US 6363013 B1	Auto-stopped page soft-programming method with voltage limited component	365/185.18	17	20020326
5	☐	☐	US 6335882 B1	Nonvolatile semiconductor memory device capable of erasing blocks despite variation in erasing characteristic of sectors	365/185.29	34	20020101
6	☐	☐	US 6230233 B1	Wear leveling techniques for flash EEPROM systems	711/103	15	20010508
7	☐	☐	US 5671178 A	Erase verifying circuit for a nonvolatile semiconductor memory with column redundancy	365/185.22	18	19970923